

**Features:**

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications:

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V _{RRM} , V _{DRM}	Type & Outline		
	2000V	MTx400-20-405F3	MFx400-20-405F3
2200V	MTx400-22-405F3	MFx400-22-405F3	
2500V	MTx400-25-405F3	MFx400-25-405F3	
2500V	MT400-25-405F3G		

MTx stands for any type of **MTC**, **MTA**, **MTK**

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Single side cooled, T _c =55°C	125			400	A
I _{T(RMS)}	RMS on-state current					628	A
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	125			45	mA
I _{TSM}	Surge on-state current			125		11	kA
I ² t	I ² t for fusing coordination	V _R =60%V _{RRM} , t=10ms half sine,	125			605	10 ³ A ² s
V _{TO}	Threshold voltage			125		0.82	V
r _T	On-state slope resistance					0.79	mΩ
V _{TM}	Peak on-state voltage			25		2.18	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =67%V _{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t _r ≤0.5μs Repetitive	125			200	A/μs
I _{GT}	Gate trigger current	V _A =12V, I _A =1A	25	30		200	mA
V _{GT}	Gate trigger voltage			0.8		3.0	V
I _H	Holding current			10		200	mA
I _L	Latching current					1000	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =67%V _{DRM}	125			0.20	V
R _{th(j-c)}	Thermal resistance Junction to case	Single side cooled per chip				0.11	°C/W
R _{th(c-h)}	Thermal resistance case to heatsink	Single side cooled per chip				0.04	°C/W
V _{iso}	Isolation voltage	50Hz, R.M.S, t=1min, I _{iso} :1mA(MAX)		3000			V
F _m	Terminal connection torque(M12)			12		14	N·m
	Mounting torque(M6)			4.5		6	N·m
T _{vj}	Junction temperature			-40		125	°C
T _{stg}	Stored temperature			-40		125	°C
W _t	Weight				1060		g
Outline		405F3					

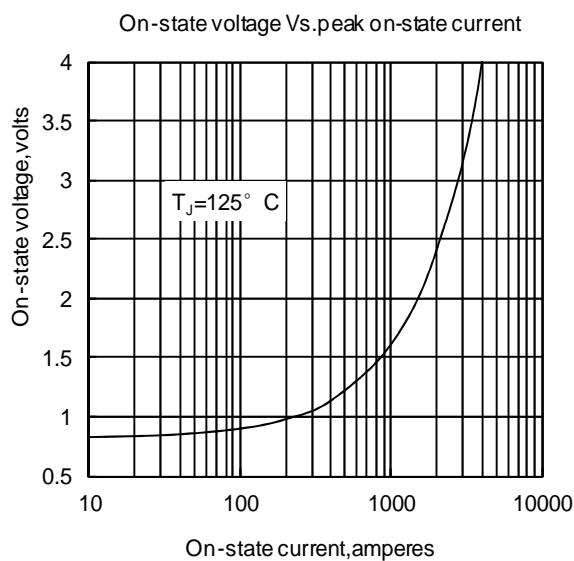


Fig1

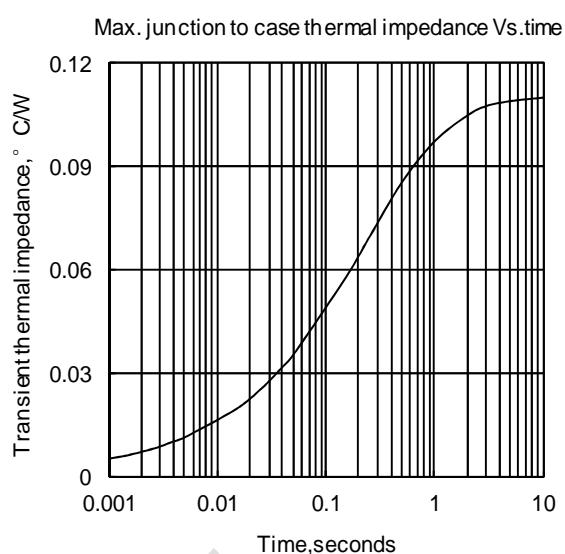


Fig2

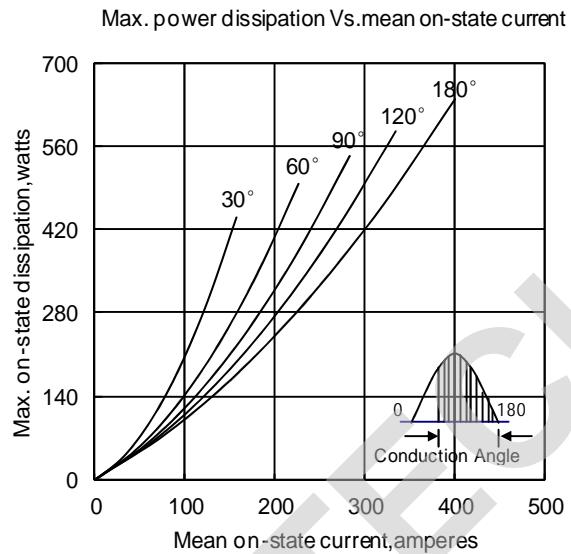


Fig3

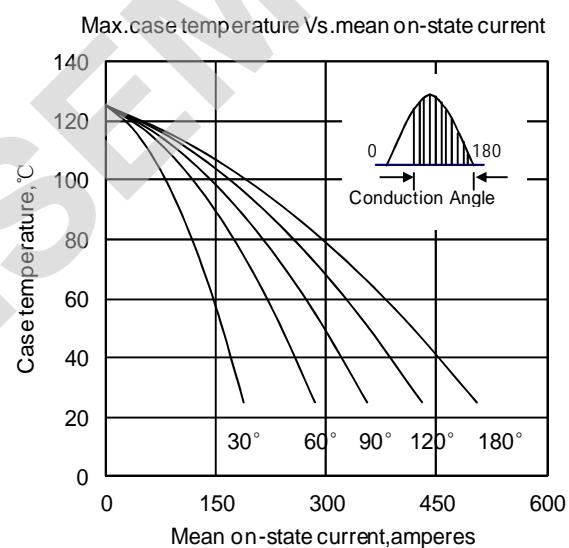


Fig4

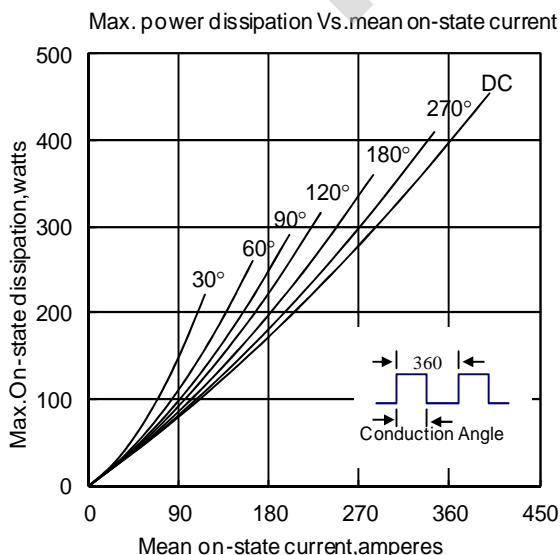


Fig5

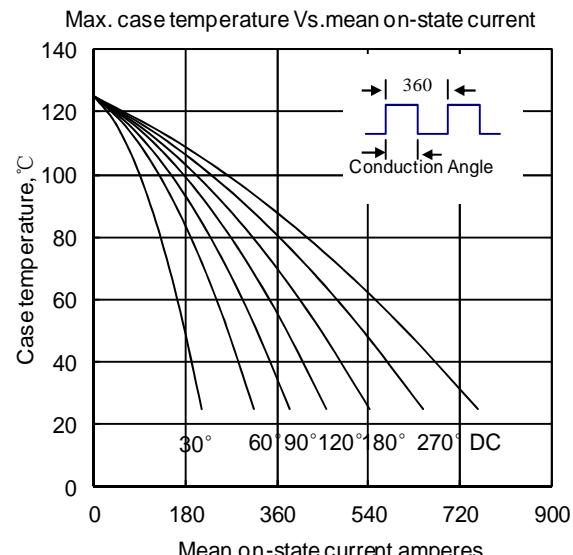


Fig6

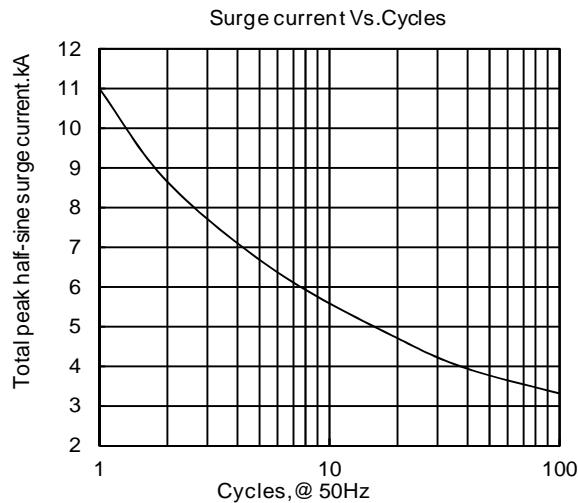


Fig 7

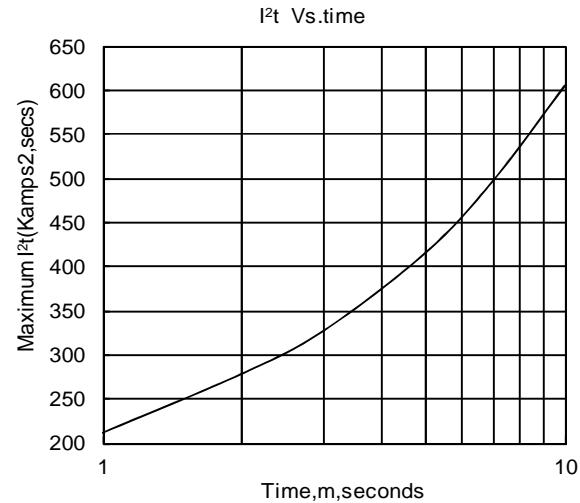


Fig 8

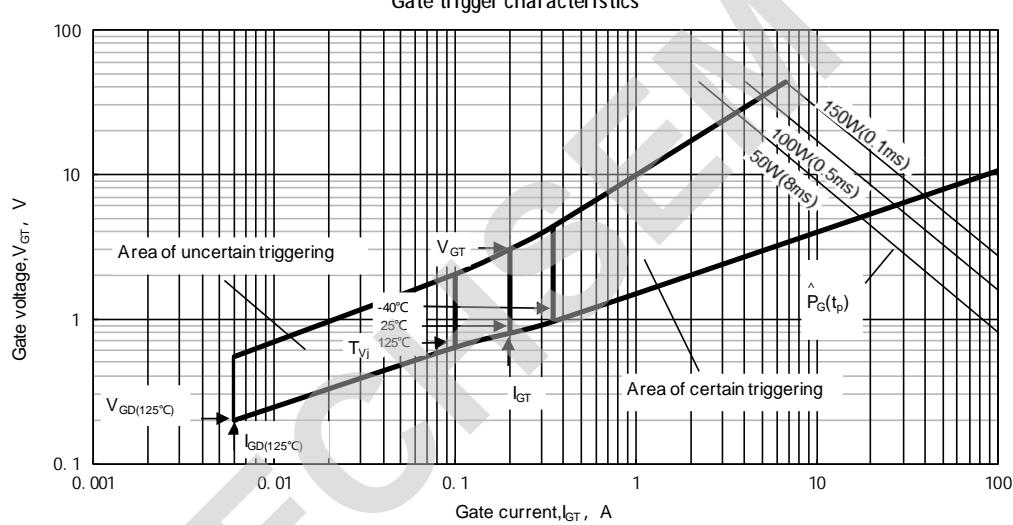
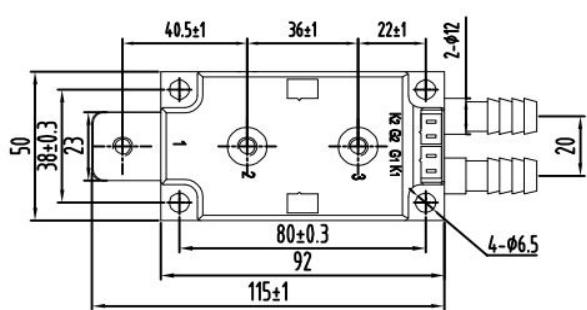
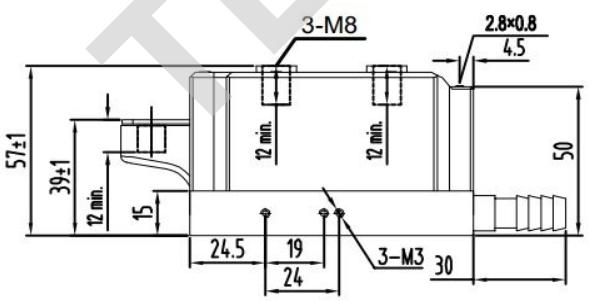


Fig.9

Outline:**Unmarked dimensional tolerance: ±0.5mm**